Thunderbolt Interconnect—Opitcal and Copper

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***Abstract*—Thunderbolt interconnect technology has adopted copper and optical cables. Single cable can support 2 × 20 Gb/s data rate, which is driven by 4K video. Future 8K video and virtual reality will push the bandwidth requirement even higher. Key technologies developed to enable this high data rate for consumer electronics are discussed, such as robust copper and optical cables, miniature optical engine, and 2 × 25.625 Gb/s low power integrated circuits for vertical cavity surface emitting laser based optical link. Copper and optical interconnect technologies are compared on the basis of cost, power, form factor, and scalability. Same circuit with four channels (4 × 25.625 Gb/s) can be used in 100G data center optical interconnect. Total power consumption is 146 mW for each 25.625 Gb/s optical link, which gives 5.69 mW/Gb/s. Among the commercially available optical ICs we evaluated at 25 Gb/s, this work has lowest power consumption and smallest die area in industry.**

***Index Terms*—BiCMOS, optical interconnect, optical transceiver, thunderbolt, vertical cavity surface emitting laser (VCSEL), 100 Gb/s.**

I. Introduction

INTERCONNECT technology has progressed at a very fast pace in the past decade. The signaling rate has steadily increased from 100 Mb/s to 25 Gb/s. With the release of Thunderbolt technology, we are entering a new era in consumer electronics that runs at 20 Gb/s line rate (40 Gb/s throughput per connector interface) [1], [2]. This is driven by the bandwidth requirements of the 4K video, which quickly become the main stream today. Since 8K video and Virtual Reality (VR) are already on the horizon, significant jump in interconnect throughput is required down the road. On the data center and cloud side, mobile data traffic is contributing more than 50%, and the percentage is still increasing. This pushes data center interconnect data rate to 100G, 400G and higher. Electrical I/O is increasingly limited by copper channel, whose interconnect loss is frequency and distance dependent. To overcome this limitation, extra circuitry has been added to compensate for copper channel's loss; these circuits burn more power, add more complexity and take extra spaces [2], [3]. On the other hand, optical fiber has been widely used over longer distances while maintaining higher data rate due to significantly lower attenuation and better immune to electro-magnetic interference (EMI). In addition, with smaller and smaller system form factors, there is not much room left for all the connectors, such as Ethernet, eSATA, DVI, USB, HDMI and Display Port [2], [3]. Thunderbolt (TBT) interconnect technology was introduced to the market around late 2011, it is the new high-speed, low power, small form factor cable technology, with the intension to be the single universal I/O for future computers and portable devices.

Fig. 1. Thunderbolt cable. Copper cable on the left, optical cable on the right.

Thunderbolt interconnect technology has introduced two types of active cable: copper and optical, as shown in Fig. 1 [2]. An active copper cable supports the link distance of <3 m at 10 Gb/s, <2 m at 20 Gb/s. An active Vertical Cavity Surface Emitting Laser (VCSEL) based optical cable supports link distance up to 60 m. In the next generation Thunderbolt cable (Gen 3), 2 × 20 G Thunderbolt signal and 10G USB3.1 signal are converged to the same USB type-C connector. The introduction of the optical cable technology in the Thunderbolt opens up new usage models previous not allowed by the copper cables in consumer electronics [1].

II. Challenges and Design

One of the design challenges was to make the IC small enough to fit into the miniature optical engine which fits inside the regular cable plug. At 25 Gb/s, total integrated noise is higher than at 10 Gb/s due to higher bandwidth, this puts higher challenge on receiver sensitivity requirement. In general, bipolar has higher gain than CMOS per gain stage, and ∼1–2 dB better noise performance [7]. In this design, BiCMOS process was chosen in order to have less gain stages and compact high speed channel, while the advantage of CMOS still exists for integrating digital control, power management and VCSEL biasing control circuitry. In this work, 0.18 μm BiCMOS was chosen to save tape out and wafer manufacturing cost.

Another challenge is to make the optical cable robust enough to handle daily consumer abuses. In the past few years, Intel has been working on robust optical cable, which can handle staple gun test, flexing and twisting, hard pinch, even hammer drop test, and the fiber inside the cable does not break.

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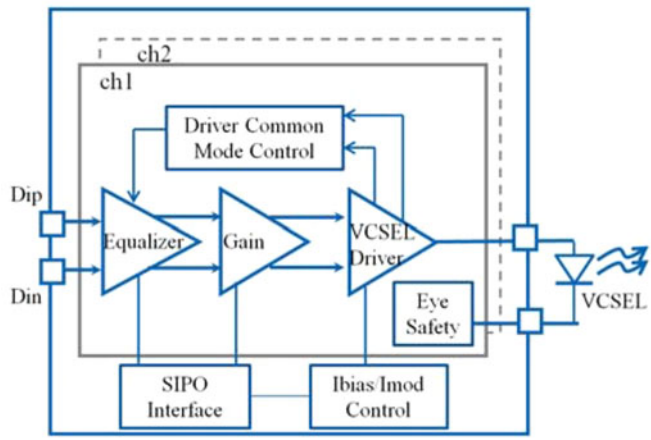

Fig. 2. 2 × 25G transmitter block diagram.

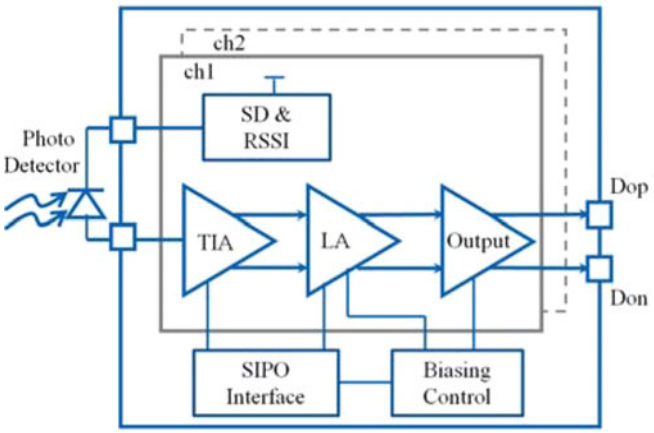

Fig. 3. 2 × 25G receiver block diagram.

Fig. 2 shows the 2 × 25.625G transmitter (TX) IC block diagram. It has two identical channels, each channel consists of high speed signal path (input equalizer, gain stage, VCSEL driver), low speed serial-in-parallel-out (SIPO) control interface, VCSEL bias and modulation current control, eye safety, and driver common mode voltage feedback control.

Fig. 3 is 2 × 25.625G receiver (RX) IC block diagram. Each channel has high speed signal path (Trans-Impedance Amplifier (TIA), limiting amplifier (LA), output stage), SIPO, biasing control, signal detect (SD) & receiver signal strength indicator (RSSI).

Fig. 4 shows TX detailed circuit. Electrical input swing is 200mV differential peak-to-peak. Q1 and Q2 form input stage along with the emitter degeneration which gives ∼3 dB equalization capability. Low speed driver common mode control loop ensures that Q3 and Q4 are operating at the right DC bias voltage over Process Voltage & Temperature (PVT). Dummy VCSEL & Filter block minimize large current spike on power supply while keeping node A an AC ground. Eye Safety and Cathode Switch form a protection which ensures VCSEL is off if the anode voltage is too high (e.g. bonding wire shorted to power supply).

RX detailed circuit is shown in Fig. 5. Q1 and Q2 form a single-ended TIA, which is powered by on-chip regulator. Q3,

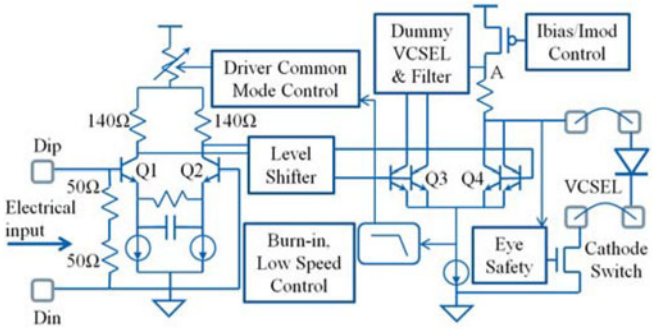

Fig. 4. Transmitter circuit.

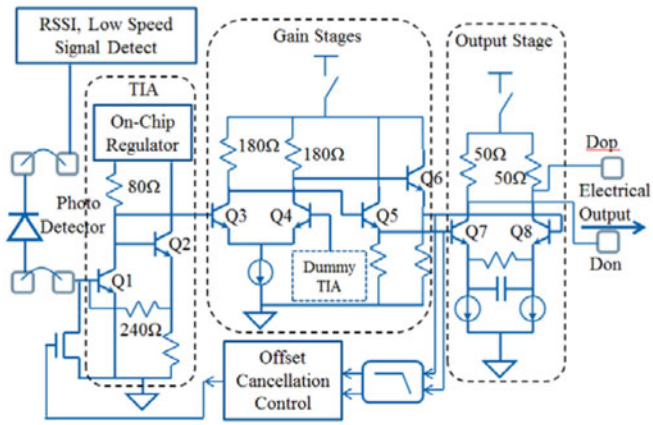

Fig. 5. Receiver circuit.

Q4, Q5, Q6 form a gain stage, whose gain is around 13 dB. Output stage has 2∼3 dB pre-emphasis capability. Low speed offset cancellation control loop removes the average current from the photo detector (PD). Electrical output swing is 200 mV differential peak-to-peak.

At 25 Gb/s, there are re-timers in the electrical signal path and they are <1.5 inches away from optical IC electrical interface. In order to reduce power consumption and have a compact design, TX has only one gain stage. Thanks to the high gain of bipolar, high speed signal can fully switch diff-pair Q3/Q4 with only one gain stage. 77% TX power is consumed by VCSEL itself, only 23% power is consumed by gain stage. Testing result shows that one gain stage and 3 dB equalization in TX is sufficient in the optical link. Fig. 6 shows TX input equalizer normalized gain simulation plot.

On RX side, output swing is ∼200 mV. RX's 2–3 dB output equalization can compensate the 1.5-inch PCB loss, before the signal reaches the re-timer.

III. Measurement Results

The measurement vehicle used in this work is a standard QSFP28 100G optical module. Since we have both 2-channel and 4-channel ICs (all channels are identical), we tested 4-channel 4 × 25.625G TX and RX. Fig. 7 shows the chip micrograph, where TX is wire bonded to VCSEL array, RX is wire bonded to photo detector (PD) array [2]. Fig. 8 is a QSFP28 optical module PCB board, where the 4 × 25G optical engine is

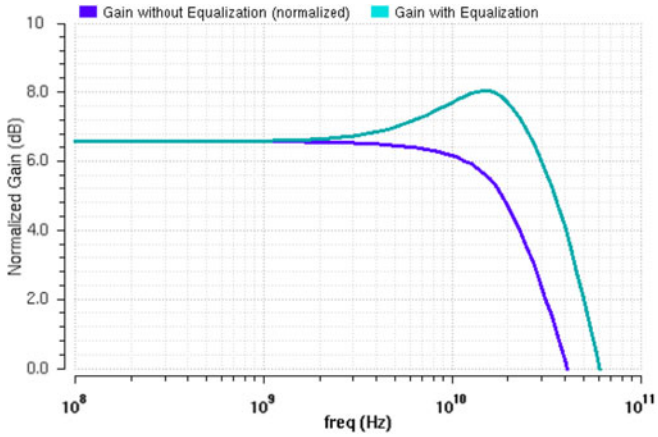

Fig. 6. TX input equalization.

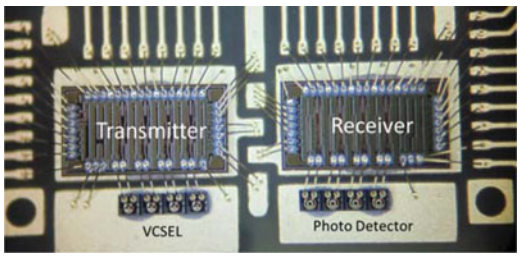

Fig. 7. 4 × 25G TX and RX chip micrograph.

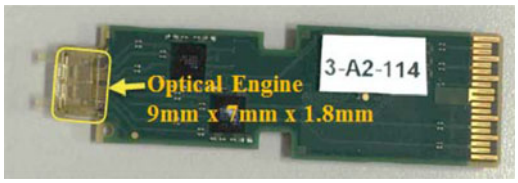

Fig. 8. 4 × 25G optical engine on PCB.

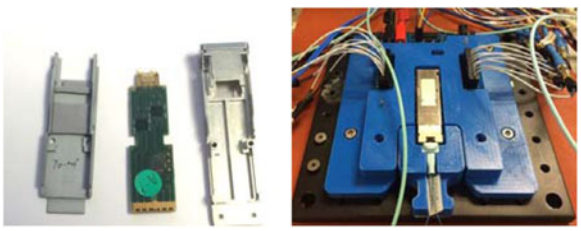

Fig. 9. Optical module PCB, housing, and test setup.

caped under the yellow plastic lens. The whole optical engine is very small, 9 mm × 7 mm with 1.8 mm height. The two black squares are the re-timers.

Fig. 9 shows QSFP28 optical module PCB and housing on left side, and the test setup on right side. At 25.625 Gb/s, TX VCSEL light output eye diagrams are shown in Fig. 10 [2]. At 35 °C total jitter is 12 ps, and eye height is 620 uW. At 70 °C, total jitter is 13 ps, eye height is 514 uW. Two optical eyes were measured at the same VCSEL current biasing condition.

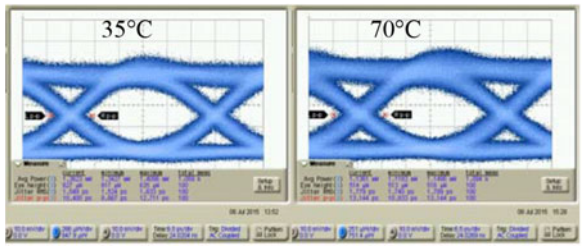

Fig. 10. VCSEL output eye diagram at 35 °C and 70 °C.

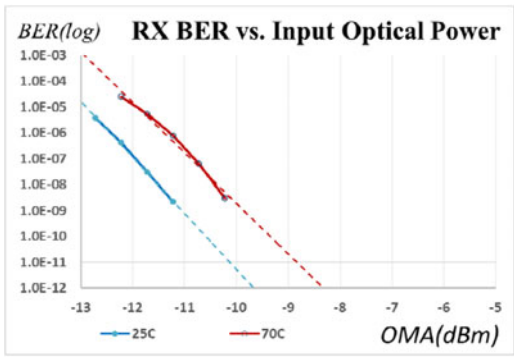

Fig. 11. RX BER measurement result.

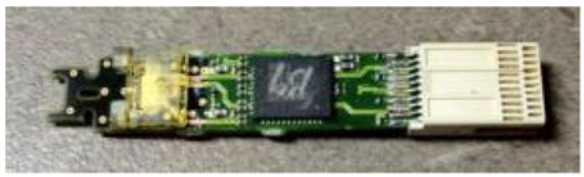

Fig. 12. Thunderbolt optical cable paddle board.

At higher temperature, VCSEL's slope efficiency and bandwidth are degraded, the eye has more closure.

Fig. 11 is the RX Bit-Error-Rate (BER) measurement results. Photo detector's responsivity is 0.5 mA/mW. From the extrapolation (dashed lines), RX optical modulation amplitude (OMA) sensitivity (BER = 1.0E-12) is −9.7 dBm and −8.4 dBm at 25 °C and 70 °C, respectively. Due to PCB layout restriction, RX electrical output eye were not measured. At higher temperature, RX's bandwidth drops and circuit noise increases, this makes RX's sensitivity worse at higher temperature.

Transmitter VCSEL launching power is about 1.3 dBm (OMA). The optical link margin (BER = 1.0E-12) is 11 dB at 25 °C, and 9.7 dB at 70 °C. With this large link margin, 1E-15 BER is achieved, without using sophisticated equalization and forward-error-correction (FEC). The worst case optical coupling loss at TX and RX side is 2 dB.

Fig. 12 shows current generation (Gen 2) Thunderbolt optical cable paddle board, which resides inside the connector plug shown in Fig. 1 (black plug). The optical engine has very similar design as in Fig. 8, but smaller size (5 mm × 6 mm × 1.8 mm) [2], [3].

Fig. 13 is a new miniature Thunderbolt optical engine, which has 2 × 25G optical ICs, VCSEL/PD and optical lens inside.

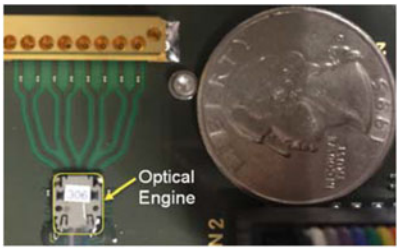

Fig. 13. Miniature thunderbolt optical engine.

TABLE I
OVERVIEW OF MEASUREMENT RESULTS

Technology	0.18 μm BiCMOS
Power supply	3.3 V
Optical wavelength	850 nm
Date rate	2 × 25.625 Gb/s(2-channel) 4 × 25.625 Gb/s(4-channel)
Optical link margin	11.0 dB @25 °C 9.7 dB @70 °C
RX sensitivity (OMA)	–9.7 dBm @25 °C –8.4 dBm @70 °C
Transmitter power	68 mW
Receiver power	78 mW
Total power dissipation	146 mW per 25G link
Total die size	2 × 1.11 mm^2

The dimension of the optical engine is 8.2 mm × 6 mm × 1.7 mm, it can go through reflow soldering process, and fit into the Thunderbolt optical cable connector plug [2].

The measurement results are summarized in Table I.

IV. ADVANTAGES

Compared with prior publications of 10–25 Gb/s optical link ([3]–[8]), and copper interconnects, this design has the following advantages:

Power: At 10 Gb/s, Thunderbolt Gen 2 Optical-to-Electrical (O/E) conversion power per optical link was ∼13.4 mW/Gb/s [3]. As of today, copper link's power performance bench mark is ∼15–25 mW/Gb/s [1], and the power is mainly used to overcome signal degradation from the high attenuation of copper cable, which is ∼7 dB per meter. Optical fiber has very low attenuation (∼2 dB per kilometer), which allows longer reach optical cable. At 25 Gb/s, Intel's Thunderbolt optical engine (VCSEL-based) has achieved O/E conversion power efficiency of ∼ 5.69 mW/Gb/s, thanks to the compact IC design and low power consumption of VCSEL (∼15 mW at 25 Gb/s). This low power made the optical engine design small enough to fit into the regular cable plug without the heat sink.

Form Factor: Miniature optical transceiver is critical to achieve the small form factor required inside the cable plug. In order to achieve that, the ICs have very compact design and are highly integrated with digital serial interface, VCSEL temperature sensor, biasing current compensation control, power management circuitry, etc. Total IC area for 2-channel 25 Gb/s optical link (TX + RX) is 2.22 mm^2. VCSEL also has very small die size (∼ 250 μm × 250 μm per VCSEL, shown in Fig. 7).

TABLE II
COMPARISON OF THREE DIFFERENT CABLE TECHNOLOGIES

Technology	Copper	Optical-SiP	TBT Optical-VCSEL
Cost	↑	↘	↗
Distance	↓	↑	↗
Power	↑	↘	↗
Form Factor	↑	↘	↗
Scalability	↓	↗	↗

A single-piece precision molded plastic lens covers the VCSEL, PD, and optical ICs, and provides efficient optical coupling from fibers to optical devices. The size of the whole optical engine is 5 mm × 6 mm × 1.8 mm, small enough to fit into the TBT cable plug.

On cable side, based on the Thunderbolt electrical cable products, the signal conditioning chip is used to make the copper cable thinner, instead of longer, and consumer always prefers to have thin and light cable [1]. To make this happen, very small copper wires (AWG38, AWG40) are used. These extremely thin copper wires have high attenuation and very limited reach. Since the optical fiber is thinner and lighter than the copper counterpart, the cable form factor definitely favors the optics.

Cost: For consumer electronics, cost is extremely sensitive, and low cost is the key to market success. Traditionally, optical transceiver assembly cost is high due to precision optical alignment. This optical engine's planar single-piece lens design made the assembly process fully automatic possible with the fast precision die bonding and lens attachment. Along with the compact low power ICs, this new optical engine design has really driven down the cost of the optical transceiver. Similar optical engine design shown in Fig. 8 for QSFP28 will further drive down cost of data center optical links.

On cable side, optical fiber is significantly cheaper than the copper wire counterpart assuming the same length. However, additional cost is added into active optical cable due to the optical engine (O/E conversion) and the fiber cable termination [1]. In a short cable (∼1 m), the raw copper cable cost is a small portion of the total cost, therefore the fixed cost adder of the optical engine makes the active optical cable more expensive. However, as the cable gets longer, the cost advantage of optical cable starts to shine. As a rough estimation (assume similar volume on both copper and optical cable), the crossover point is ∼3–5 m. For consumer interconnects, the volume on copper cable is still much bigger than that of the optical cable. As the data rate goes higher, this crossover point will get shorter.

Table II shows a comparison of three different cable technologies beyond 25 Gb/s: active copper cable, Silicon Photonics based optical link (optical-SiP) and VCSEL-based TBT optical link. For short distance, copper is the winner. Silicon Photonics

based optical link is for much longer distance, cost is relatively higher due to more sophisticated modulation scheme and 3-D die stack packaging. In between 5 meters and a few hundred meters, VCSEL based optical link is the best solution. In the future, silicon photonics integration with modulator may drive down the cost, but VCSEL-based optical link is still the cheapest based on current commercially available optical links and market shares.

V. Conclusion

This work demonstrates 2 × 25.625 Gb/s low power optical transmitter and receiver ICs, and the latest Thunderbolt optical interconnect technology. 4 × 25.625 Gb/s optical transmitter and receiver ICs can be used in 100G QSFP28 optical link in data center application. This 25 Gb/s optical link has lowest power consumption, smallest form factor, lowest cost among alternative options available in industry, and achieved 11 dB optical link margin for BER of 1.0E-12 without using forward-error-correction (FEC). High link margin and high bandwidth VCSEL will make Pulse Amplitude Modulation (PAM-4) very possible at 50 Gb/s (25 Gbaud/s).

Based on Thunderbolt cable products, copper and optical interconnect technologies will co-exist in the foreseeable future. Copper serves the short reach link while optics expands link distance for various new usage models, such as Virtual Reality. Cost, power and form factor will determine either copper or optics being used in a specific usage model. We do expect the reach cross-over point between copper and optics to become shorter and shorter as data rates go up. At 20 Gb/s, this length has reduced to ∼3 m. As the high-speed VCSEL technology advances, optical cable will be well positioned in the next generation Thunderbolt interconnect technology and other consumer I/O, and can be further scaled to 50G, 100G and higher data rate.

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Authors' biographies not available at the time of publication.